Amendments to the Specification:

Please replace paragraph [0015] on page 5 with new paragraph [0015] as follows:

[0015] Achieving the same access timing for all memory commands is accomplished by performing a complete row access operation for every read, write and refresh command received. The complete row access operation includes word line assertion, memory cell readout, bit line sensing, cell content restoration, word line deassertion, and bit line equalization and precharge. The following description illustrates the implementation details that permit memory devices or memory macro blocks fabricated using conventional DRAM process technology to perform data accesses with latency and cycle times similar to page accesses performed by conventionally architected DRAMs. However, the present architecture is not dependent on the pattern in which the memory is accessed ~~as is the previous technology~~.